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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/591,216	06/09/2000	Giora Biran	6727/OH271	2935

7590 02/20/2004
Darby & Darby PC
805 Third Avenue
New York, NY 10022

EXAMINER

NEURAUTER, GEORGE C

ART UNIT	PAPER NUMBER
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2143

DATE MAILED: 02/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/591,216

Applicant(s)

BIRAN ET AL.

Examiner

George C Neurauter, Jr.

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 31 December 2003.
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-24 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) 1-24 is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-24 have been considered but are moot in view of the new ground(s) of rejection.

In regards to the Applicant's argument that Moyal does not teach an arbiter wherein the logic circuitry is of a size that is substantially independent of the number of clients served by the arbiter and that there is limited discussion of physical implementation, the Examiner does not agree. Moyal discloses as cited in the previous Office Action:

"Each network equipment device has means by which several sources of input data may be destined to the same destination... The control means that is utilized in many devices is called an arbiter." (column 2, lines 10-12 and 15-16)

Moyal also discloses:

"The arbiter can be easily implemented in various networking products that handle large numbers of input sources (queues, ports, etc.)" (column 4, lines 25-27)

One of ordinary skill in the art knows that an ATM switch as disclosed in Moyal (column 1, lines 57-64), known to be implemented strictly in hardware or in a "physical implementation", has a plurality of input ports that may receive data from an unknown amount of clients sending requests. If the arbiter was to be implemented in such a router to accept requests from an unknown amount of clients, the logic circuitry would have to be independent of the number of clients served by it because there is no way

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the arbiter can know the number of clients it will serve. Therefore, Moyal meets the limitation and the Examiner sustains the rejection.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

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5. Claims 1-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moyal et al. (US Patent 6 445 680 B1) in view of Lau et al. (US Patent 5 893 162 A).

Regarding claim 1, Moyal discloses an arbiter which arbitrates between a plurality of clients generating requests for access to a resource in a computing environment, comprising:

a memory, comprising for each of the plurality of clients: a next-client pointer, which is adapted to record an identification of another one of the clients making a subsequent request to access the resource, so as to form a linked list of the requests; and

logic circuitry which is adapted to decide, responsive to the linked list, which of the plurality of clients is given access to the resource. (column 2, line 10-column 3, line 41; column 4, line 6-column 5, line 39, specifically column 4, lines 57-column 5, line 6 and column 5, lines 12-19)

Moyal does not disclose wherein a memory, comprising for each of the plurality of clients, a request register, which is adapted to record a number of the client's access requests or logic circuitry which is adapted to update the linked list in response to the number of access requests of each of one or more of the clients, however, Moyal does disclose a memory, comprising for each of the plurality of clients: a request register, which is adapted to record the respective client's access requests [column 2, line 10-column 3, line 41; column 4, line 6-column 5, line 39].

Lau discloses the above limitations (column 5, lines 5-32, specifically lines 13-18 and 29-31; column 7, lines 44-column 8, line 10, specifically column 8, lines 54-58; column 8, lines 10-67, specifically lines 30-32 and 45-50)

Lau discloses that the request register ("block counter") is used by the logic circuitry ("managing RAM" or "management RAM") to provide VLSI control of ATM data into and out of a shared memory that contains the linked list (column 1, line 66-column 2, line 3; column 2, lines 4-13).

Based on the specific advantages described above in Lau regarding the use of a request register and logic circuitry and wherein a nexus exists such that the references are both directed towards using linked lists of input queues in order to accept ATM data from a plurality of sources (see column 4, lines 5-12 and 28-32 of Moyal; see column 2, lines 4-18 and column 3, lines 13-41 of Lau) and using hardware implementations of logic circuitry to decide which data is output (see column 2, lines 10-12 and 15-16 and column 4, lines 25-27 of Moyal; see column 1, lines 14-21 and column 1, line 59-column 2, line 6 of Lau), one of ordinary skill in the art would have found it obvious to combine the teachings of these references because one of ordinary skill in the art would have appreciated the specific advantages of the secondary reference and would have been directed to the references due to the nexus connecting the references.

Therefore, it would have been obvious to achieve the limitations as described in the claim.

Claim 15 is rejected since claim 15 recites a method with substantially the same limitations as recited in claim 1.

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Regarding claim 2, Moyal and Lau disclose an arbiter according to claim 1.

Moyal discloses wherein the memory comprises at least one list-terminating pointer which indicates an end of the linked list. (column 4, line 6-column 5, line 39, specifically column 4, line 57-column 5, line 6 and column 5, lines 12-39; column 6, lines 38-57)

Claim 16 is rejected since claim 16 recites a method with substantially the same limitations as recited in claim 2.

Regarding claim 3, Moyal and Lau disclose an arbiter according to claim 2.

Moyal discloses wherein the at least one list-terminating pointer comprises a tail pointer which indicates a last client in the linked list. [column 4, line 6-column 5, line 39, specifically column 4, line 57-column 5, line 6 and column 5, lines 12-39; column 6, lines 38-57]

Claim 17 is rejected since claim 17 recites a method with substantially the same limitations as recited in claim 3.

Regarding claim 4, Moyal and Lau disclose an arbiter according to claim 2.

Moyal disclose wherein the at least one list-terminating pointer comprises a head pointer which indicates a first client in the linked list, and wherein the logic circuitry is operative to decide, responsive to the head pointer, which of the plurality of clients is given access to the resource. [column 4, line 6-column 5, line 39, specifically column 4, lines 6-12, column 4, line 57-column 5, line 6 and column 5, lines 12-39; column 6, lines 38-57]

Claim 18 is rejected since claim 18 recites a method with substantially the same limitations as recited in claim 4.

Regarding claim 5, Moyal and Lau disclose an arbiter according to claim 1.

Moyal discloses wherein the logic circuitry is operative to check whether a client requesting access to the resource has a pending access request. [column 4, line 6-column 5, line 39, specifically column 4, lines 27-56 and column 5, lines 20-39]

Moyal does not disclose wherein the logic circuitry is operative to update the number of access requests of the client requesting access responsive to the check, however, Moyal does disclose wherein the logic circuitry is operative to check whether a client requesting access to the resource has a pending access request, and to update a record of the number of pending access requests recorded in the respective register responsive to the check. [column 4, line 6-column 5, line 39, specifically column 4, lines 27-56 and column 5, lines 20-39]

Lau discloses the above limitation (column 7, lines 44-column 8, line 10, specifically column 8, lines 54-58; column 8, lines 10-67, specifically lines 30-32 and 45-50).

Claim 5 is rejected since the motivations regarding the obviousness of claim 1 also apply to claim 5.

Claim 19 is rejected since claim 19 recites a method with substantially the same limitations as recited in claim 5.

Regarding claim 6, Moyal and Lau disclose an arbiter according to claim 1.

Moyal discloses wherein the logic circuitry is operative to check whether the resource is available, and to allocate the resource responsive to the check. [column 4, line 6-column 5, line 39, specifically column 5, lines 7-11 and 20-38]

Claim 20 is rejected since claim 20 recites a method with substantially the same limitations as recited in claim 6.

Regarding claim 7, Moyal and Lau disclose an arbiter according to claim 1.

Moyal does not disclose wherein an arbiter comprises at least one buffer wherein requests from a specific client are stored before the number of requests of the specific client are recorded in the request register of the specific client, however, Moyal does disclose wherein an arbiter comprises at least one buffer wherein requests from a specific client are stored before being recorded in the respective request register. [column 4, line 6-column 5, line 39, specifically column 4, line 34-column 5, line 39]

Lau discloses the above limitation (column 7, lines 44-column 8, line 10, specifically column 8, lines 54-58; column 8, lines 10-67, specifically lines 30-32 and 45-50).

Claim 7 is rejected since the motivations regarding the obviousness of claim 1 also apply to claim 7.

Claim 21 is rejected since claim 21 recites a method with substantially the same limitations as recited in claim 7.

Regarding claim 8, Moyal and Lau disclose an arbiter according to claim 1.

Moyal discloses wherein an arbiter comprises a first-in first-out memory wherein requests from the plurality of clients are stored before being transferred sequentially to

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the memory and the logic circuitry. [column 4, line 6-column 5, line 39, specifically column 4, line 34-column 5, line 39]

Regarding claim 9, Moyal discloses an arbiter according to claim 1.

Moyal discloses wherein the memory comprises:

for at least some of the clients, a priority flag which is adapted to record a priority for access to the resource for the at least some clients; and at least one list-terminating pointer for the priority, which indicates an end of the linked list for the at least some clients. [column 4, line 6-column 5, line 39, specifically column 4, lines 6-12 and column 5, lines 7-11; column 7, line 43-column 8, line 32, specifically column 7, lines 50-52]

Claim 22 is rejected since claim 22 recites a method with substantially the same limitations as recited in claim 9.

Regarding claim 10, Moyal and Lau disclose an arbiter according to claim 9.

Moyal discloses wherein the logic circuitry is adapted to decide, responsive to the linked list and the priority flag, which of the clients is given access to the resource. [column 4, line 6-column 5, line 39, specifically column 4, lines 6-12 and column 5, lines 7-11; column 7, line 43-column 8, line 32, specifically column 7, lines 50-52 and column 7, line 61-column 8, line 3]

Claim 23 is rejected since claim 23 recites a method with substantially the same limitations as recited in claim 10.

Regarding claim 11, Moyal and Lau disclose an arbiter according to claim 1.

Moyal does not disclose wherein the logic circuitry is of a size that is independent of a quantity of clients served by the arbiter, and wherein the circuitry is adapted to

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decide, responsive to the numbers of recorded requests, which of the plurality of clients is given access to the resource, however, Moyal does disclose wherein the logic circuitry is of a size that is substantially independent of the number of clients served by the arbiter, and wherein the circuitry is adapted to decide, responsive to the recorded requests, which of the plurality of clients is given access to the resource. [column 1, lines 57-64; column 2, lines 10-12 and 15-16; column 3, line 42-column 4, line 3; column 4, line 6-column 5, line 39, specifically column 4, lines 6-12 and 23-51]

Lau discloses the limitations above [column 3, line 42-column 4, line 3; column 4, line 6-column 5, line 39, specifically column 4, lines 6-12 and 23-51; column 10, lines 5-56]

Claim 11 is rejected since the motivations regarding the obviousness of claim 1 also apply to claim 11.

Claims 13 and 24 are rejected since claims 13 and 24 recite an arbiter and method with substantially the same limitations as recited in claims 1 and 11 in combination.

Regarding claim 12, Moyal and Lau disclose an arbiter according to claim 1.

Moyal discloses wherein a size of the memory scales as a product of the number of clients and a logarithm of the number of clients. [column 3, line 42-column 4, line 3; column 4, lines 6-51]

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US Patent 5 408 463 A to Merchant et al;

US Patent 6 046 982 A to Ozveren et al;

US Patent 6 625 122 B1 to Joffe;

US Patent 6 633 568 B1 to Han et al;

US Patent 6 667 984 to Chao et al;

Badran et al. "Head of Line Arbitration in ATM Switches with Input-Output Buffering and Backpressure Control", Global Telecommunications Conference, 1991 (GLOBECOM '91: Countdown to the New Millennium), 2-5 Dec 1991, pages 347-351, vol.1.

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

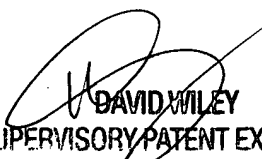
A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to George C Neurauter, Jr. whose telephone number is 703-305-4565. The examiner can normally be reached on Monday-Saturday 5:30am-10pm Eastern.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Wiley can be reached on 703-308-5221. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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